



LCD Module Specification

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2.0 Record of revision

Rev	Date	Item	Page	Comment



3.0 General specification

Display format: 2 x 40

Character size: 5 x 7

View area: 154.9 x 16.3

General dimensions: 182 x 33.5

LCD type: STN Gray STN Yellow FSTN

Polarizer mode: Reflective Transflective
 Transmissive Negative

View angle: 6 O'clock 12 O'clock Others_____

Backlight: LED EL CCFL

Backlight colour: Yellow green Amber Blue green
 White Others

Controller/Driver: KS0066U (controller/driver) and KS0063B (driver)

Temperature range: Normal temperature Wide temperature
Operating 0 to 50 C Operating -20 to 70 C
Storage -20 to 70 C Storage -30 to 80 C

**4.0 Absolute maximum rating** $V_{SS} = 0V, T_a = 25^{\circ}C$

NO	ITEM	SIMBOL	MIN	MAX	UNIT
1.	Power Supply voltage (Logic)	$V_{DD} - V_{SS}$	0	7	V
2.	Power Supply voltage (LCD Driver)	$V_{DD} - V_0$	-	12	V
3.	Operating Temperature	T_{op}	Refer page 3		$^{\circ}C$
4.	Storage Temperature	T_{st}	Refer page 3		$^{\circ}C$

5.0 Electrical characteristics

NO	ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
1.	Power Supply voltage (Logic)	$V_{DD} - V_{SS}$	-	2.75	-	5.5	V
2.	Power Supply voltage (V_{LCD})	$V_{DD} - V_0$	$25^{\circ}C$	4.3	4.5	4.7	V
3.	Input Voltage (except OSC1)	V_{IH}	-	$0.7V_{DD}$	-	V_{DD}	V
		V_{IL}	-	-0.3	-	0.6	V
4.	Current Supply	I_{DD}	$V_{DD} - V_{SS} = 5V$	-	5	-	mA

6.0 Environmental requirements

NO	ITEM	CONDITION
1.	Operating Temperature	Refer page 3
2.	Storage Temperature	Refer page 3
3.	Operating Humidity	5% to 95%RH
4.	Cycle Test	0 C @ 30 min to 50 C @ 30min for 1 cycle run for 10 cycles

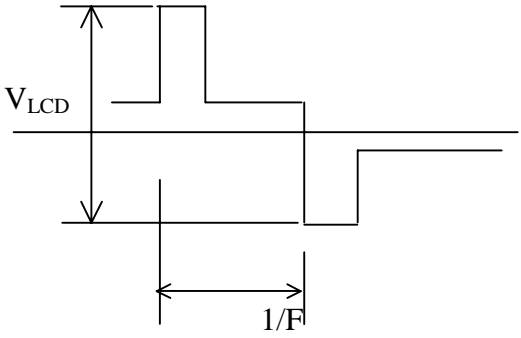
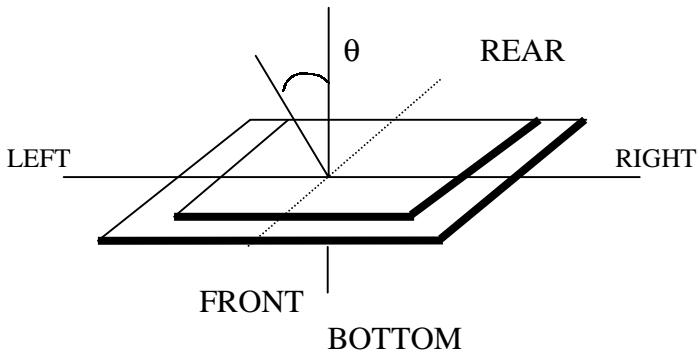
Note: The background on LCD has the possibility to be changed in different temperature range.



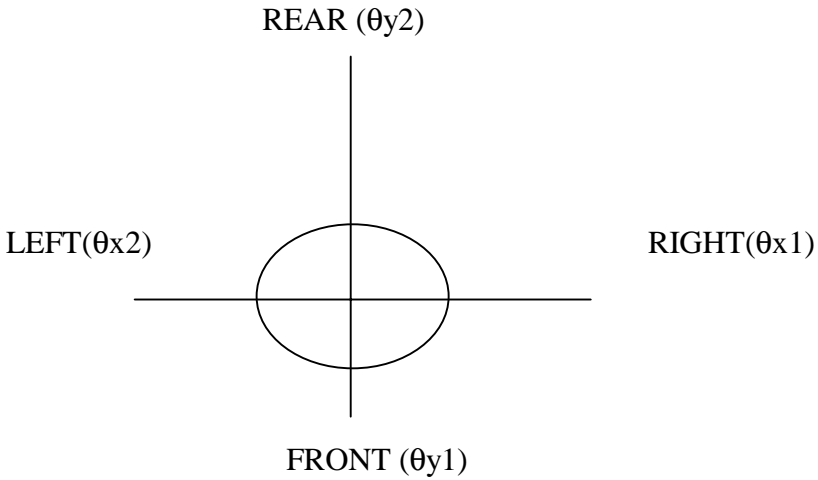
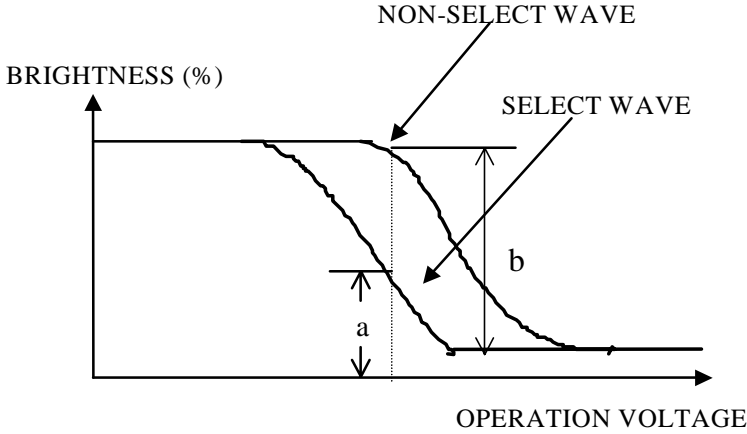
7.0 LCD specification

7.1 Electro-optical characteristics

NO	ITEM	SYMBOL	TEMP. °C	CONDITION	COMMERCIAL			UNIT	REF.
					MIN	TYP	MAX		
1	Operating Voltage	V_{LCD}	25	$\theta = 0$ $Cr = \max$	4.3	4.5	4.7	Volt	7.1.1
2	Viewing	$\theta_x 1$	25	$CR \geq 2$ $V_{LCD} = 4.5V$	-	45	-	Deg	7.1.2
		$\theta_x 2$			-	45	-		
		$\theta_y 1$			-	50	-		
		$\theta_y 2$			-	45	-		
3	Contrast Ratio	Cr	25	$\theta = 0^\circ, V_{LCD} = 4.5V$	-	10	-		7.1.3

NO	CHARACTERISTICS	DEFINITIONS
7.1.1	Definition of Operating Voltage (V_{LCD})	 <p>V_{LCD} : Operating Voltage F : Frame Frequency</p>
7.1.2	Definition of Viewing Angle	 <p>LEFT RIGHT FRONT BOTTOM REAR</p>



		
<p>7.1.3</p>	<p>Definition of Contrast Ratio</p>	 <p>Contrast Ratio = $\frac{\text{Brightness of non-selected state (b)}}{\text{Brightness of selected state (a)}}$</p> <p>Conditions</p> <ul style="list-style-type: none">(a) Operating Voltage: V_{LCD}(b) Temperature: $25^{\circ}C$(c) Viewing Angle, $\theta = 0^{\circ}$

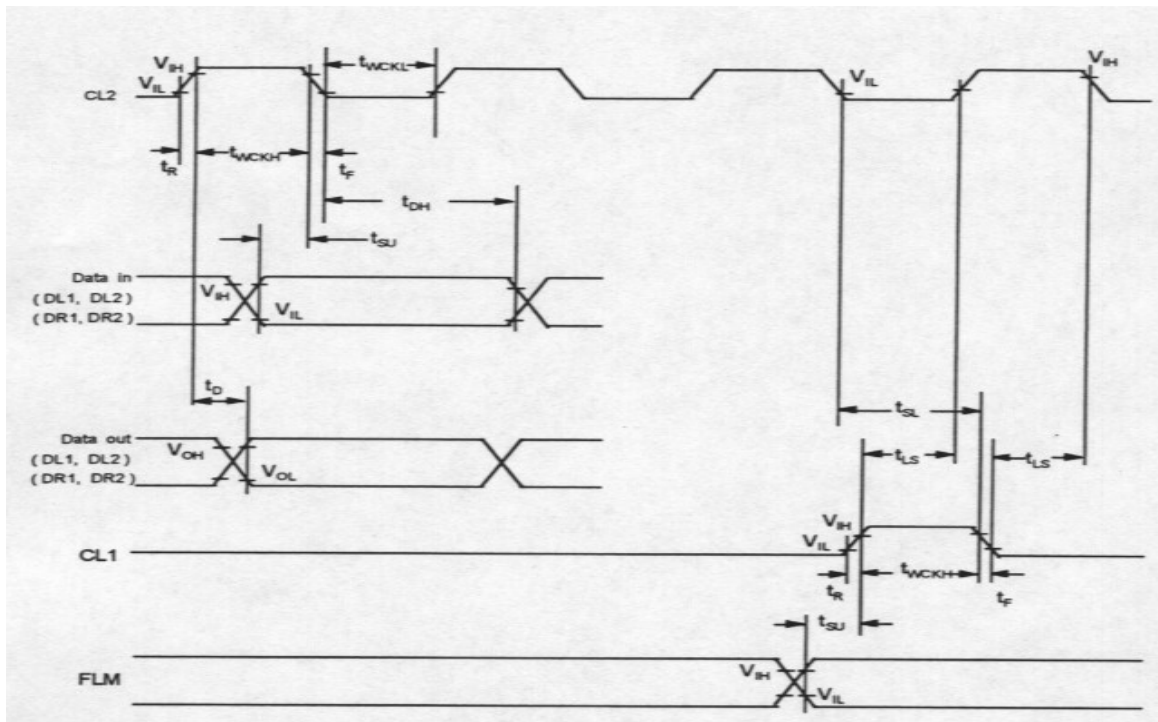


8.0 Interface

8.1	Display Driver	KS0066U and KS0063B	
8.2	Duty Cycle	1/16	
8.3	Pin-out Assignments		
	Pin No	Symbol	Description
	1	V _{SS}	Ground terminal of module
	2	V _{DD}	Supply terminal of module
	3	V _O	Power supply for Liquid Crystal Drive
	4	RS	Register Select: RS = 0 Instruction Register RS = 1 Data Register
	5	R/W	Read/Write: High = Read Low = Write
	6	E	Enable
	7 to 14	D0 to D7	Bi-directional Data Bus. Data Transfer is performed once, thru D0 to D7, in the case of interface data length is 8-bits.
	15	(BL -)	LED power supply terminals
	16	(BL +)	

9.0 TIMING CHARACTERISTICS/TIMING DIAGRAMS

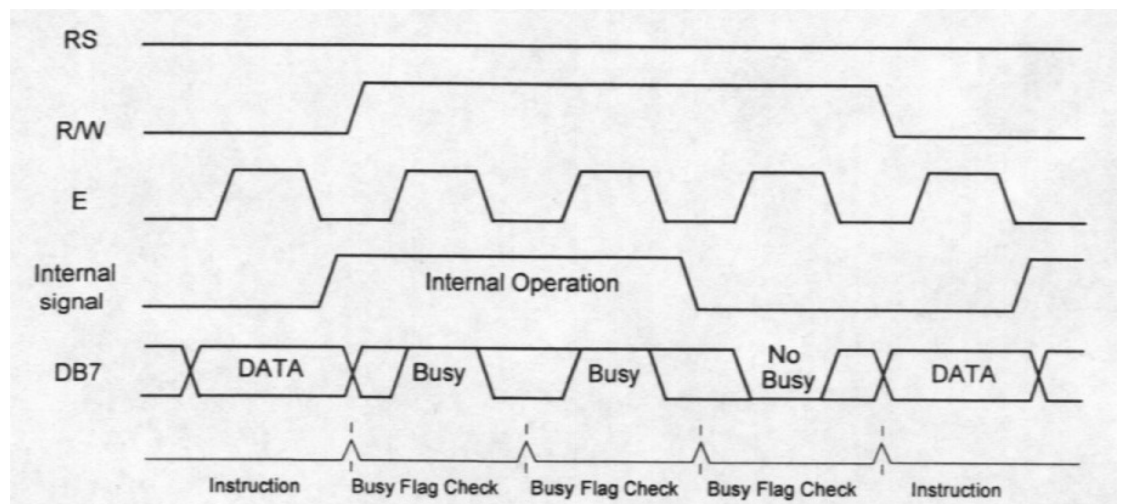
9.1 Timing Characteristics for KS0063B



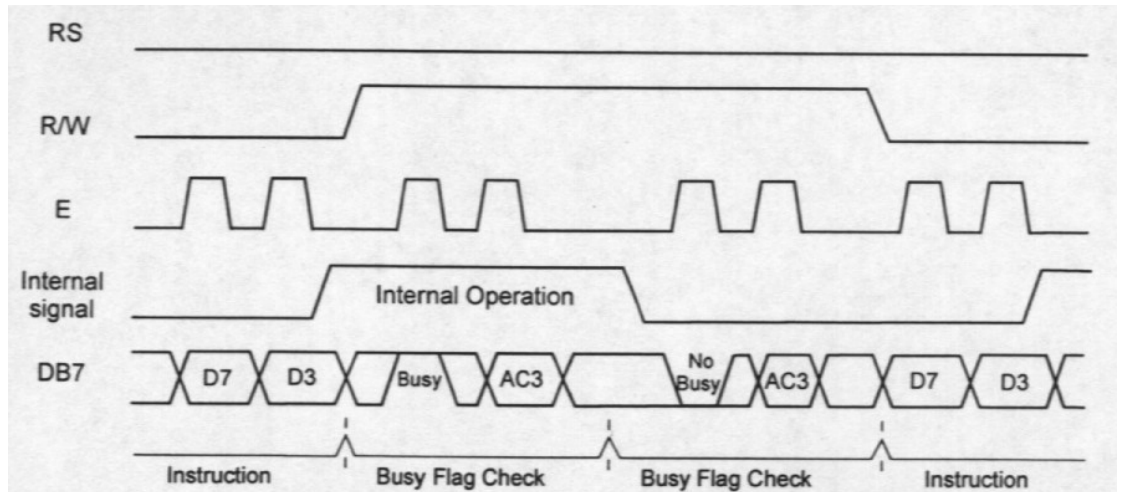


Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Data shift frequency	f_{CL}	-	-	400	KHz	CL2
Clk high level width	t_{WCKH}	-	800	-	ns	CL1, CL2
Clk low level width	t_{WCKL}	-	800	-		CL2
Clk setup time	t_{SL}	From CL2 to CL1	500	-		CL1, CL2
	t_{LS}	From CL1 to CL2	500	-		
Clk rise/fall time	t_R/t_F	-	-	200		
Data setup time	t_{SU}	-	300	-		DL1, DL2, DR1, DR2
Data hold time	t_{DH}	-	300	-		
Data delay time	t_D	$C_L = 15pF$	-	500		

9.2 Timing Characteristics for KS0066U

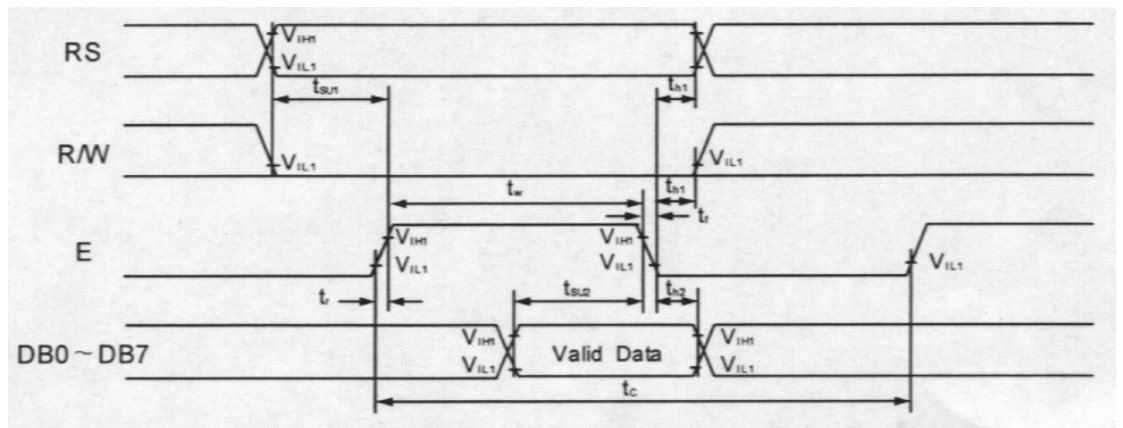


Example of 8-bit Bus mode timing diagram



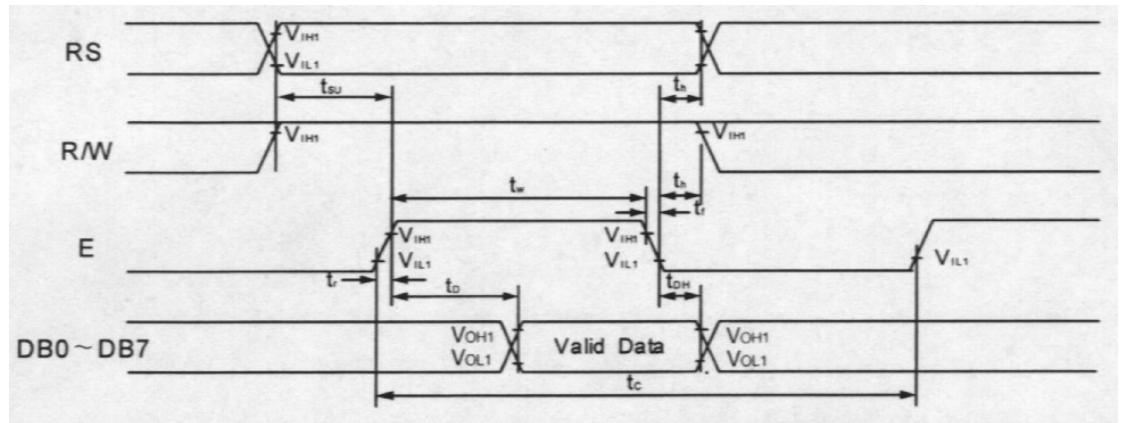
Example of 4-bit Bus mode timing diagram

9.3 Timing Diagrams for Write Mode and Read Mode (KS0066U)



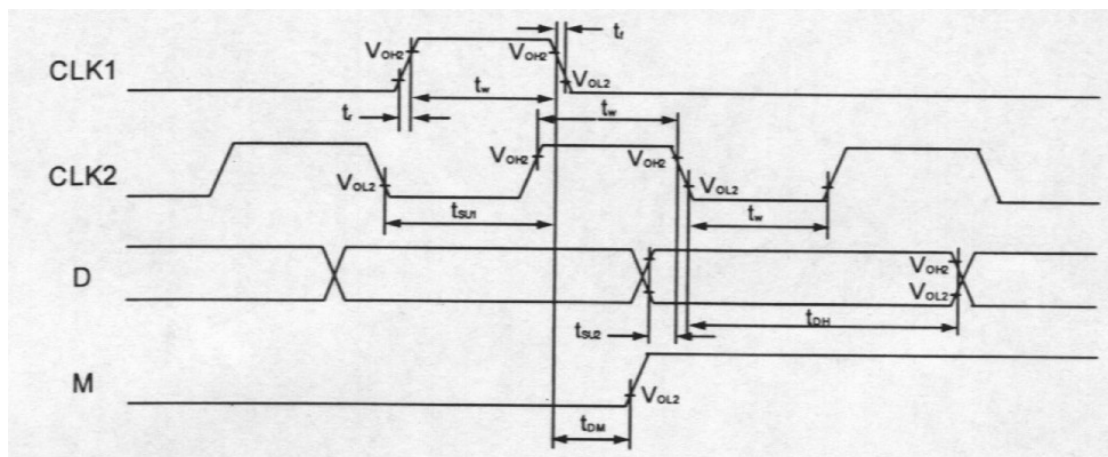
Write Mode Timing Diagram

Item	Symbol	Condition	Min	Max	Unit
Enable cycle time	t_c	$V_{DD} = 4.5$ to $5.5V$ $T_a = -30$ to $+85C$	500	-	ns
Enable rise/fall time	t_r, t_f		-	20	
Enable pulse width (high, low)	t_w		230	-	
R/W and RS setup time	t_{su1}		40	-	
R/W and RS hold time	t_{h1}		10	-	
Data setup time	t_{su2}		80	-	
Data hold time	t_{h2}		10	-	



Read Mode Timing Diagram

Item	Symbol	Condition	Min	Max	Unit
Enable cycle time	t_c	$V_{DD} = 4.5$ to $5.5V$ $T_a = -30$ to $+85C$	500	-	ns
Enable rise/fall time	t_r, t_f		-	20	
Enable pulse width (high, low)	t_w		230	-	
R/W and RS setup time	t_{su1}		40	-	
R/W and RS hold time	t_{h1}		10	-	
Data setup time	t_{su2}		-	120	
Data hold time	t_{h2}		5	-	



Interface mode with extension driver timing diagram

Item	Symbol	Condition	Min	Max	Unit
Clock pulse width (high, low)	t_w	$V_{DD} = 2.7$ to $4.5V$ $T_a = -30$ to $+85C$	800	-	ns
Clock rise/fall time	t_R, t_F		-	25	
Clock setup time	t_{SU1}		500	-	
Data setup time	t_{SU2}		300	-	
Data hold time	t_{DH}		300	-	
M delay time	t_{DM}		-1000	1000	



Relationship between character code (DDRAM) and character pattern (CGRAM)

Character Code (DDRAM data)								CGRAM Address							CGRAM Data								Pattern number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0		
0	0	0	0	x	0	0	0	0	0	0	0	0	0	x	x	x	0	1	1	1	0	pattern 1	
											0	0	1					0	0	0			
											0	1	0					0	0	0			
											0	1	1					1	1	1	1		
											1	0	0					1	0	0	0		
											1	0	1					1	0	0	0		
											1	1	0					1	0	0	0		
											1	1	1					0	0	0	0		
0	0	0	0	x	1	1	1	0	0	0	0	0	0	x	x	x	1	0	0	0	1	pattern 8	
											0	0	1					0	0	0			
											0	1	0					0	0	0			
											0	1	1					1	1	1	1		
											1	0	0					1	0	0	0		
											1	0	1					1	0	0	0		
											1	1	0					1	0	0	0		
											1	1	1					0	0	0	0		

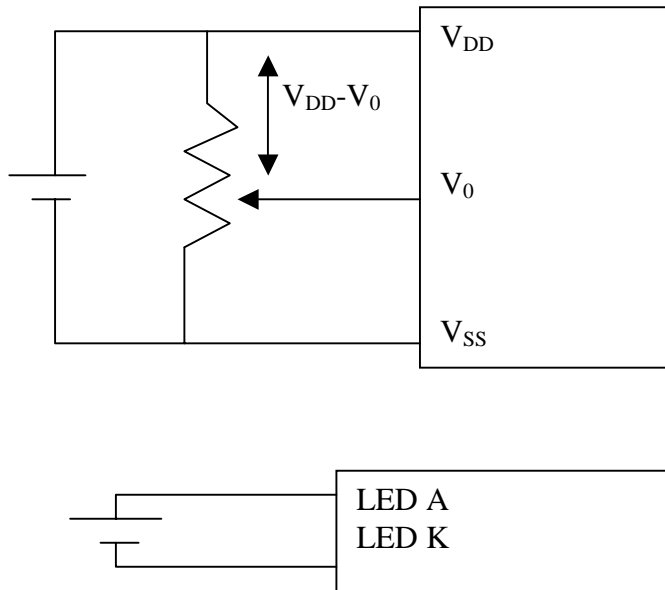


Character Generator ROM (KS0066)

Upper 4bit / Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
LLLH	(2)	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
LLHL	(3)	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
LLHH	(4)	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
LHLL	(5)	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
LHLH	(6)	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
LHHL	(7)	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
LHHH	(8)	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
HLLL	(1)	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
HLLH	(2)	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
HLHL	(3)	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
HLHH	(4)	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
HHLL	(5)	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
HHLH	(6)	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
HHHL	(7)	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]
HHHH	(8)	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]	[Pattern]

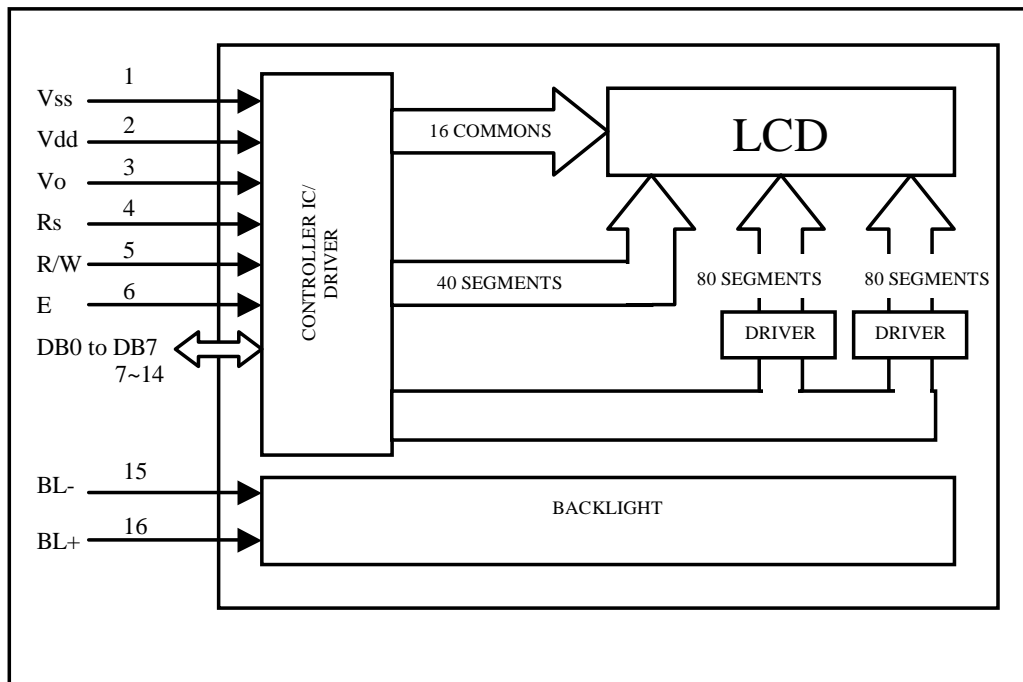


10. Power Supply



Where $V_{DD}-V_0 = \text{LCD Driving voltage}$

11. Block Diagram





12. Instructions

Instruction	Code										Description	Executed time(max) fosc=270KHz	
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
Clear Display	0	0	0	0	0	0	0	0	0	0	1	Clear all display and returns the cursor to the home position (Address 0)	1.53 ms
Cursor at home	0	0	0	0	0	0	0	0	0	1	*	Returns the cursor to the home position (Address 0). Also return the display being shifted to the original position. DDRAM contents remain unchanged.	1.53 ms
Entry mode set	0	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies or not to shift the display. These operations are performed during data write and read.	39 μs
Display on/off control	0	0	0	0	0	0	0	1	D	C	B	Sets the ON/OFF of all display (D) cursor ON/OFF (C), and blink of cursor position character (B).	39 μs
Cursor/display shift	0	0	0	0	0	0	1	S/C	R/L	*	*	Moves the cursor and shifts the display without changing the DDRAM contents.	39 μs
Function set	0	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (N) and character font (F).	39 μs
CGRAM address set	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0		Sets the CGRAM, data is sent and received after this setting.	39 μs
DDRAM address set	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0		Set the DGRAM, data is sent and received after this setting.	39 μs
Busy Flag/ address read	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0		Recall Busy flag (BF) indicating internal operation is being performed and read address counter contents.	0 μs
CGRAM/DDRAM data write	1	0	WRITE DATA									Writes data into DDRAM or CGRAM	43 μs
CGRAM/DDRAM data read	1	1	READ DATA									Reads data into DDRAM or CGRAM	43 μs

Code	Description	Executed time (max)
I/D=1: Increment I/D=0: Decrement S=1: With display shift S/C=1: Display shift S/C=0: Cursor movement R/L=1: Shift to the right R/L=0: Shift to the left DL=1: 8-bit	DL= 0:4-bit 1/16 duty 1/8 duty, 1/11 duty F= 1:5x10 dots F= 0: 5x7 dots BF=1: Internal operations is being performed BF=0: Instruction acceptable	DDRAM: Display Data RAM CGRAM: Character Generator RAM ACG: CGRAM Address ADD: DDRAM Address Corresponds to cursor address AC: Address Counter, used for both DDRAM and CGRAM *: Invalid
		Fcp or fosc = 250KHz However, when frequency changes, execution time also changes. Example If fcp or fosc is 270KHz



8 bit operation, 8 digit 2line display example.

Step	Instruction											Display	Operation
No	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
1	Power supply on												Initialized. No display
2	Function set 0 0 0 0 1 1 1 0 X X												Sets to 8 bit operation and select 2 lines display and 5x8 dot character font.
3	Display on/off control 0 0 0 0 0 0 1 1 1 0											-	Turn on display and cursor. All display is in space mode because of initialisation.
4	Entry mode set 0 0 0 0 0 0 0 1 1 0											-	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CGRAM. Display is not shifted.
5	Write data to CGRAM/DDRAM 1 0 0 1 0 0 0 0 1 1											C_	Writes C. DDRAM has already been selected by initialisation when the power was turned on. The cursor is incremented by one and shifted to the right.
6													
7	Write data to CGRAM/DDRAM 1 0 0 1 0 1 0 0 1 0											CRYSTAL CLEAR_	Writes R
8	Set DDRAM address 0 0 1 1 0 0 0 0 0 0											CRYSTAL CLEAR_	Sets DDRAM address so that the cursor is positioned at the head of the second line.
9	Write data to CGRAM/DDRAM 1 0 0 1 0 1 0 1 0 0											CRYSTAL CLEAR T_	Writes T
10													
11	Write data to CGRAM/DDRAM 1 0 0 1 0 0 1 0 0 0											CRYSTAL CLEAR TECH_	Writes H
12	Entry mode set 0 0 0 1 0 0 0 1 1 1											CRYSTAL CLEAR TECH_	Sets mode to shift display at the time of write.
13	Write data to CGRAM/DDRAM 1 0 0 1 0 1 1 0 0 1											CRYSTAL CLEAR TECHNOLOGY	Writes Y. Display is shifted to the left. The first and second lines both shift at the same time.
14													
15	Return home 0 0 0 1 0 0 0 0 1 X											CRYSTAL CLEAR TECHNOLOGY	Returns both display and cursor to the original position (address 0)